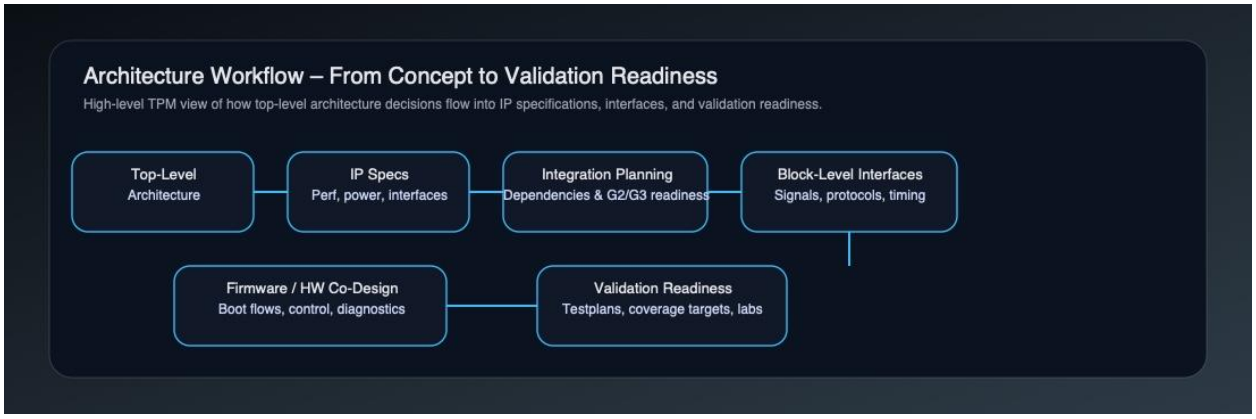
NVIDIA-Style Technical Program Manager Case Study

GPU Architecture & Accelerator SoC Scenario

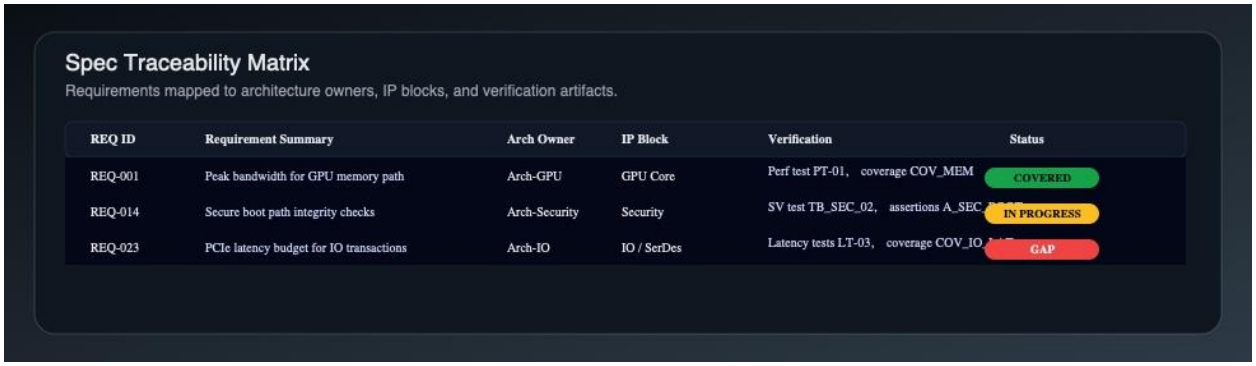
This case study focuses on a hypothetical GPU accelerator SoC program. As TPM, the emphasis is on coordinating graphics and compute IP, interconnect fabrics, and memory subsystems while ensuring verification, performance, and power goals remain on track.

Objective	TPM Actions
Unify GPU & AI Accelerator Requirements	• Run cross-team requirement workshops to align GPU, AI, memory, and interconnect needs. • Maintain an architecture decision log to capture tradeoffs, assumptions, and approvals. • Ensure requirement stability across feature changes and performance targets.
Coordinate IP Delivery Across Global Sites	• Track IP readiness across distributed design teams and time zones. • Identify schedule risk early and drive mitigation with IP owners. • Ensure interface change management and dependency alignment across compute, graphics, security, and media blocks.
Secure Verification & Performance Confidence	• Monitor functional and code coverage progress for all GPU and SoC IPs. • Track performance projections and power analysis trends from modeling teams. • Lead weekly cross-functional bug triage and testplan alignment.
Prepare for Tape-Out & Bring-Up	• Ensure sign-off criteria are met for G3/G4 gates. • Align firmware, validation, reliability, and operations teams for silicon bring-up. • Drive documentation readiness and cross-team communication to eliminate late blockers.

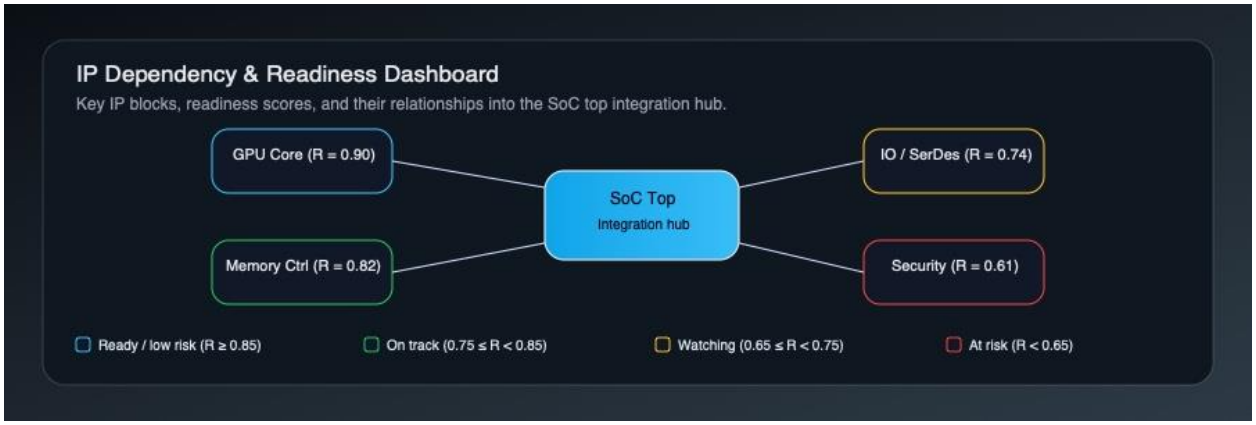
Architecture Workflow Diagram



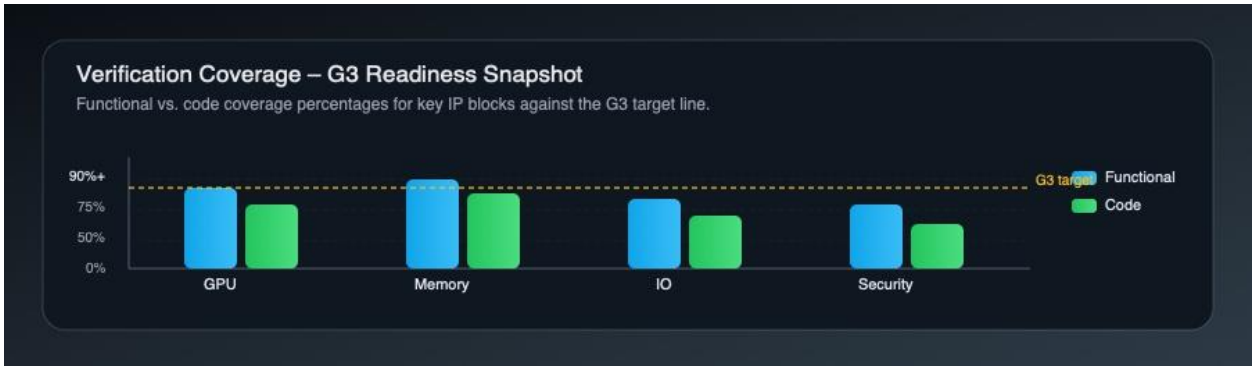
Spec Traceability Matrix



IP Dependency Dashboard



Verification Dashboard



Risk Register

This section summarizes program risks typically encountered in GPU/Accelerator SoC programs, including architectural churn, late IP delivery, verification coverage gaps, and performance/power variance. Each risk is tracked with likelihood, impact, owner, and mitigation strategy.

Risk	Likelihood / Impact	Owner	Mitigation
Late interface spec changes	Medium / High	Architecture	Establish spec freeze + decision logs
Underperforming memory subsystem	High / High	Performance	Early modeling + weekly perf reviews
Verification coverage gaps	Medium / High	Verification	Coverage dashboard + priority bug triage

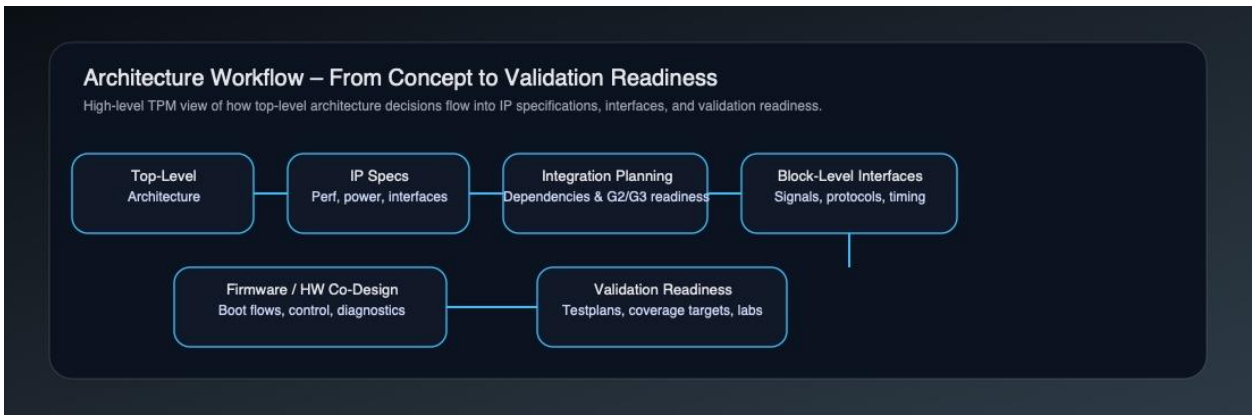
Final Outcomes

This NVIDIA-style TPM case study demonstrates how structured execution, risk visibility, and cross-team alignment directly support predictable tape-out. By enforcing architectural governance, tracking IP readiness across global teams, tightening verification signals, and coordinating bring-up preparation, the TPM role enables engineering teams to focus on technical depth while ensuring leadership receives clear, trustworthy status indicators.

Visuals by TPM Objective (Blue-Steel Views)

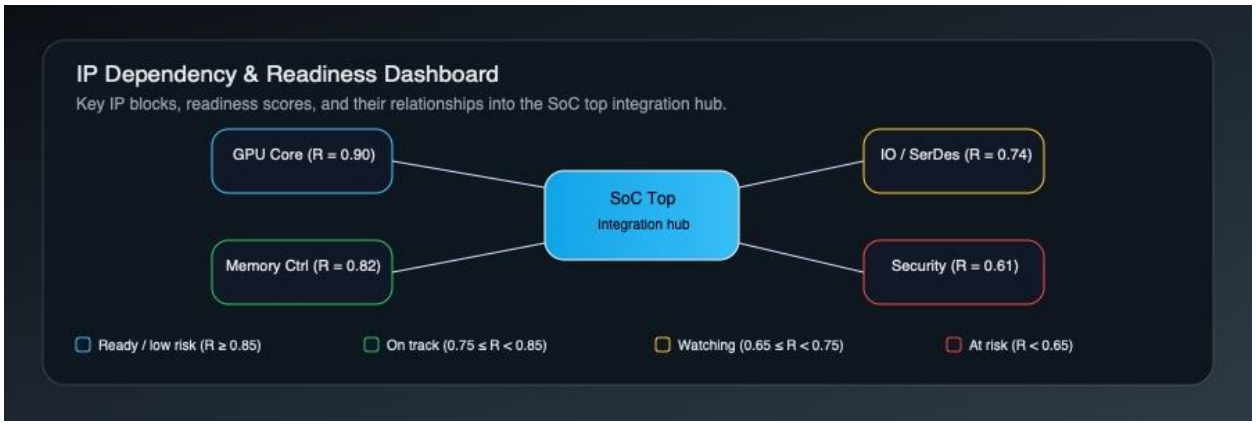
The following diagrams are aligned to each primary TPM objective in the GPU/Accelerator SoC program, making it clear how architectural decisions, IP readiness, verification confidence, and tape-out preparation are visualized.

1. Unify GPU & AI Accelerator Requirements



Architecture Workflow – from top-level GPU/AI requirements through IP specs, integration planning, block-level interfaces, firmware/hardware co-design, and validation readiness.

2. Coordinate IP Delivery Across Global Sites

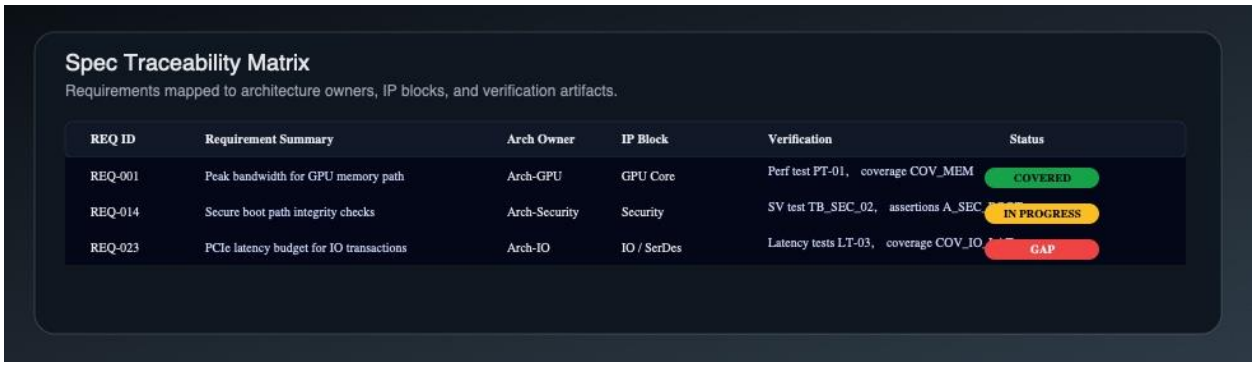


IP Dependency Dashboard – showing GPU, Memory, IO/SerDes, and Security IP readiness feeding into the SoC top, with risk-coded readiness scores.

3. Secure Verification & Performance Confidence

Verification Dashboard – coverage, bug trends, and readiness signals mapped to tape-out gates.

4. Prepare for Tape-Out & Bring-Up



Spec Traceability Matrix – linking requirements to architecture owners, IP blocks, verification artifacts, and coverage status as evidence for sign-off.