AMD Technical Program Manager Case Study

ASIC Architecture & Verification Alignment

This case study illustrates how Technical Program Management (TPM) drives predictability, risk reduction, and cross-functional alignment across architecture, RTL, verification, and physical design for a next-generation ASIC program. It summarizes core responsibilities, stage■gate expectations, and TPM■owned deliverables aligned with industry practices used by AMD, NVIDIA, and Intel.

TPM Responsibilities by Silicon Development Stage

Stage	TPM Responsibilities
Architecture	Requirements alignment, feature definition, cross-team governance, decision tracking
RTL Design	Dependency tracking, IP readiness, interface documentation, schedule management
Verification	Coverage tracking, testplan reviews, bug triage synchronization
Physical Design	Timing closure risk tracking, synthesis dependencies, milestone assurance
Tape-Out	Gate readiness, sign-off documentation, program reporting and escalation

This sample case study can be expanded with verification dashboards, architectural decision logs, IP readiness scoring models, and cross-functional review frameworks.